REMARKS

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, claims 1-16 have been cancelled and are replaced by new claims 17-28. Applicant would like to point out that while this application was initially filed with claims 1-12, a Preliminary Amendment was filed with this application inadvertently amending entirely different claims 1-16. While in the current Office Action, the Examiner examined the original claims 1-12, in order to avoid any confusion, Applicant has elected to cancel all of the claims (1-16) and proceed with new claims 17-28 which substantially correspond to original claims 1-12 (having been amended for clarity).

The Examiner has rejected claims 1 and 2 (now claims 17 and 18) under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,052,295 to Buchschacher et al. The Examiner has further rejected claim 3 (now claim 19) under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of U.S. Patent 6,986,151 to Lenssen et al. In addition, the Examiner has rejected claims 4-7 (now claims 20-23) under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of Lenssen et al., and further in view of U.S. Patent 5,567,976 to Dierschke et al. Furthermore, the Examiner has rejected claims 8 and 9 (now claims 24 and 25) under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of Lenssen et al. and Dierschke et al., and further in view of U.S. Patent Application Publication No. 2002/0172070.

The Buchschacher et al. patent discloses a cascade of voltage multipliers, which, as noted by the Examiner, includes "an electronic circuit comprising conversion means (see Fig. 1 and col 1 lines65-67) for converting an input voltage (U_i, col 2 line 4) into an output voltage (U_o, col 2 line 14), comprising at least a first energy storage means (a first capacitor C1, col 2 line 55) and a second energy storage means (output capacitor C_{out}, col 4 line 6) and switching means (Sw1, Sw2, Sw3, Sw4 and Sw5, Fig. 2) for periodically coupling said energy storage means (C1, C2) to one another under the control of a clock signal so as to store energy in the energy storage means (C1, C2) and transferring at least a portion of the stored energies between the energy storage means".

As noted in MPEP §2131, it is well-founded that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The subject invention, as claimed in claim 1, includes the limitation "clock signal generating means for generating the clock signals, said control signal generating means keeping the clock signals in holding states during a holding period during operation,

said holding states being equal to the states of the respective clock signals immediately before the holding state".

The Examiner has indicated that this is taught by Buchschacher et al., and states "(instead of programming the desired clock input signals the invention also makes it possible to automatically generate the desired clock input signal. For this, monitoring means must be coupled between the output OP of the voltage converter and an input of the means, col 2 lines 31-36), characterized in that the clock signal is kept in a holding state during a holding period (R_T) during operation, which holding state is equal to the state of the clock signal immediately before the holding state (The clock signals can be programmed to a part of the voltage multiplier to a non-active state, see Abstract)."

Applicant submits that the Examiner is mistaken. In particular, Buchschacher et al., at col. 2, lines 31-40, states:

> "However, instead of programming the desired clock input signals s1, d1-sn, dn, the invention also makes it possible to automatically generate the desired clock input signals s1, d1-sn, dn. For this, monitoring means MN must be coupled between the output OP of the voltage converter and an input of the means SL, as is indicated in FIG. 1. The monitoring means MN measures the difference between the output voltage U_o and the input voltage Ui in order to take a decision about the required number N of active voltage multipliers VM1-VMN."

It should be apparent from the above that Buchschacher et al. is generating the control signals such that an appropriate number of voltage multipliers are active based on a comparison of the difference between the output voltage and the input voltage.

As described in the subject specification on page 8, lines 7-13, if the input voltage is intermittent for holding periods RT, the control signals need to be generated differently. In the case of Buchschacher et al., the control signals would be changed to de-activate all of the voltage multipliers. Instead, in the subject invention, as claimed, the clock signals are placed into holding states during the holding period, wherein the holding states are "equal to the states of the respective clock signals immediately before the holding state".

With regard to this limitation, the Examiner offers a part of what Buchschacher et al. states in the Abstract. In particular, the Examiner states "The clock signals can be programmed to a part of the voltage multiplier to a non-active state, see abstract". However, this indicates that the clock signals may turn off one or more of the voltage multipliers. Applicant submits that as described above, turning off a voltage multiplier requires that the control signals be changed. In the subject invention, during the holding period, the clock signals are placed into holding states, wherein the holding states are "equal to the states of the respective clock signals immediately before the holding state".

The Lenssen et al. patent discloses an information carrier, apparatus, substrate, and system, in which an information carrier is provided with a storage unit, an integrated circuit and a coupling element. However, Applicant submits that Lenssen et al. does not provide that which is missing from Buchschacher et al., i.e., "clock signal generating means for generating the clock

signals, said control signal generating means keeping the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding state".

The Dierschke et al. patent discloses a position sensing photosensor device, in which an integrated circuit includes photosensitive sensors. However, Dierschke et al. does not supply that which is missing from Buchschacher et al. and Lenssen et al., i.e., "clock signal generating means for generating the clock signals, said control signal generating means keeping the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding state".

The Arimoto et al. patent publication discloses a semiconductor memory device, which teaches "teaches even if the voltage of the storage node of the memory cell storing the H level data drops during the data holding period, the amount of outflow electric charges is sufficiently small if the capacitance of junction capacitance C_j is sufficiently small." This indicates that the if the outflow electric charges is sufficiently small, the memory cell may continue to operate. However, Applicant does not see the relevance of this in relation to the limitations of claim 24, i.e., "the length of the holding period corresponds by approximation to that of a time period during which the photosensitive sensor does not receive a substantial quantity of light". This defines the time period of the holding states of the

conversion means. Because the memory cell may still operate during the data holding period is irrelevant to the determining of the holding period of the claimed invention.

Further, Applicant submits that Arimoto et al. does not supply that which is missing from Buchschacher et al. in view of Lenssen et al. and Dierschke et al., i.e., "clock signal generating means for generating the clock signals, said control signal generating means keeping the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding state".

In view of the above, Applicant believes that the subject invention, as claimed, is neither anticipated nor rendered obvious by the prior art, either individually or collectively, and as such, is patentable thereover.

Applicant believes that this application, containing claims 17-28, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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